Europäisches Patentamt
European Patent Office
Office européen des brevets

Bescheinigung Certificate Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

02077553.2

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
Application no.: 02077553.2
Demande no:

Anmeldetag:
Date of filing: 27.06.02
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

Koninklijke Philips Electronics N.V.
Groenewoudseweg 1
5621 BA Eindhoven
PAYS-BAS

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Power converter

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

H02M3/00

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

Power converter

The invention relates to a power converter of the buck converter type.

US-A-4,524,412 discloses a prior art power converter circuit.

In a buck converter the duty cycle of the switching node is a function of output voltage and input voltage. When a large ratio between supply voltage and output voltage is applied in a buck converter very small on times of the control switch can occur. If current mode control is applied the measured inductor current at the end of the control switch on time can therefore be disturbed by parasitic components or not settled in time.

It is, inter alia, an object of the invention to provide an improved power converter circuit. To this end, the invention provides a power converter circuit as defined in the independent claims. Advantageous embodiments are defined in the dependent claims.

In this application a method is described to keep the on time of the control switch rather constant over the whole output voltage- and input voltage range. With the proposed solution the output voltage range can be made larger and smaller inductors and output capacitors can be chosen, without the need of current sensing during the sync switch stroke. Advantageously, frequency adaptation is a function of the input- and output voltage.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter. It should be noted that these embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

REPORT

Subject : detailed description for invention disclosure regarding frequenccy adaption in buck converer.

Author : Hans Halberstadt

Date report June 25 2002

INTRODUCTION

In a (multiphase) buck converter operating in current mode control the converter current is used for:

a. current mode control.

b. overcurrent protection

The inductorcurrent is usually sensed over an external senseresistor Rsense or senseFET. The parasitic capacitances or delays will disturb the sense signal considerably if the on time of the controlfet becomes very short. Therefore a minimum on time is necessary. At low outputvoltage during start-up or shorted output / overcurrent the period time then has to be increased to guarantee that the minimum on time stays above the lower limit. The invention uses the outputvoltage (and supply voltage) of the converter to determine the switching frequency, so that the on time of the control fet is kept above the minimum on time necessary for measuring the inductor current.

PRINCIPAL OPERATION AND EQUATIONS FOR A BUCK CONVERTER

In figure 1 the principal diagram is given of a Buck converter with control fet (CF), main inductor (L), synchronous switch for the sync current. (SF) and load capacitor (Cload). The controlfet current is sensed by a senseresistor Rsense.

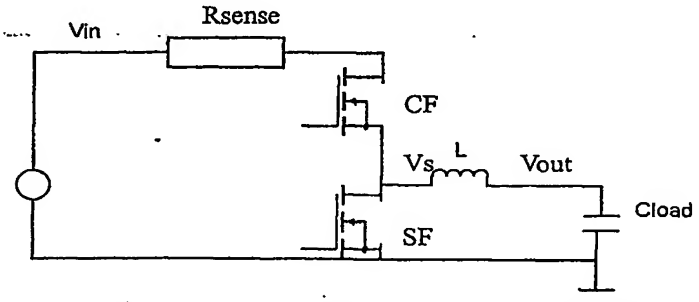

Fig 1 Buck converter principle with currentsensing in the supply line

During a converter cycle first the CF is turned on. Then the current in the inductor L rises and at a certain moment the CF is switched of and after that the SF is turned on. During the SF conduction time the inductorcurrent decreases.

When the CF is switched off on command of the current in the inductor reaching a certain level this is called current mode control.

With a buck converter operating with (direct) current mode control a minimum on time is necessary to be able to measure the current in the inductor during the control FET conduction time.

According to the basic equation of a buck converter the dutycycle (d) in steady state is a function of supply voltage and output voltage according to equation (1)

$$d = \frac{Ton}{Tper} = \frac{Vout}{Vin} \quad (1)$$

with d is the dutycycle at the switching node of a phase, Ton is the control FET conduction time and Tper is the period time of the signal at the switching node of each phase.

In case of a low output voltage for example during start up or over current protection problems can occur if Ton can not be lowered. In that case at a fixed Tper and minimum Ton the outputvoltage can not be lowered, leading to exsessive outputcurrents, destroying the switches.

If Ton can not be lower than the minimum on time (Ton min) the only possibility to be able to realize a certain output voltage at a minimum on time is to apply a period time Tper that is according to equation (1) .A longer period time is also possible,but then the system operates with a longer control fet on time leading to a larger current ripple than necessary. As the current ripple in steady state is equal to the di during the control FET stroke it can easily be seen that this ripple can be calculated as:

$$Iripple = (Vin - Vout) \cdot \frac{Ton}{L} \quad (2)$$

Therefore an optimum choice for ripple is to choose the on time as short as possible. According to (1) the minimum period time then must be :

$$Tper = Ton \cdot \frac{Vin}{Vout} \quad (3)$$

In a practical system more converters can be connected together to the same Cload. Often the timing of CF and SF of each converter is shifted over a time Tper/N if N converters are present. In this case the total ripplecurrent in the output C is further decreased. This application is called an N phase converter.

PRIOR ART

An existing method for adapting the period time is to measure the current during the sync fet conduction time and prevent the controlfet from switching on until the current in the syncFET has decreased below a certain maximum value. see US patent 4524412

An other possibility is to switch off both switches and initialize a new startup.

A third possibility is to change to dutycycle control instead of current mode control in case of low outputvoltage so that the on time can be reduced to 0 if needed.

DISADVANTAGES

an important disadvantage of the existing patent is that it is necessary to measure the current during the syncfet stroke.

This can be done without extra sensing components using the Rdson of the syncfet, but this is not very accurate, and therefore the outputcurrent can not be limited accurately in this case.

Switching off both fets and initialize a new startup is a rather crude method that only acts in emergency situations for example at shorted output.

Applying dutycycle control gives extra difficulties regarding instabilities of the control loop and possible discontinuities in the dutycycle at low dutycycles that can lead to jitter at the outputvoltage.

NEW INVENTION

A new idea is proposed where the CF on time is kept almost constant. This is realized by making the period time proportional to Vout/Vin according to equation (3)

The outputvoltage of the converter is still regulated to the desired value in a traditional way by generating an errorsignal proportional to Vout -Vref, where Vref is an internal reference value, and using this error signal to control Ton. From

equation 3 it follows that Ton will be almost constant if the relation between Tper, Vout and Vin is choosen according to equation (3) at the desired Ton.

Often Vin is fixed in the application or can have only discrete values of for example 12V or 5V. In this case it is not necessary to measure Vin accurately and it can be threated as a constant for which different values can be selected according to the actual VIN value.

A block diagram of the basic invention is given in Fig. 2. The basic invention is formed by the block "voltage to frequency converter" in combination with a standard buck converter.The converter switching frequency is adapted according to Vout/Vin (equation (3)) by a voltage to frequency converter with Vout (Vin) as input. At Vout is almost 0 or negative the frequency must be limited to a certain minimum or given a frequency offset to guarantee startup of the converter. This minimum frequency or offset will be choosen according to the desired minimum on time (maximum value of this minimum frequency) and acceptable maximum peak current.

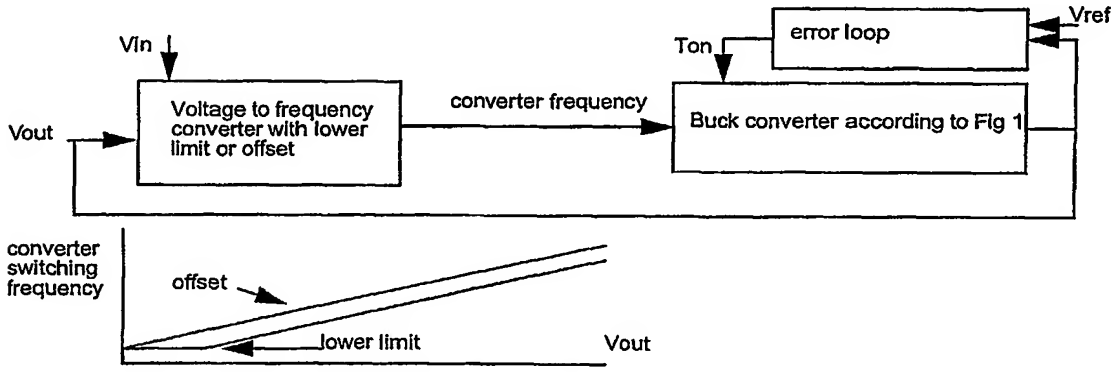

Fig 2. blockdiagram of the invention

Two implementations are given in Fig 3 and 4.

Implementation 1. Apply fixed frequency for normal operation region and lower frequency for OCP region proportional to Vout

This principle is applied in the TEA1300 and TEA1301 VRM controller IC's. In this case a fixed frequency is applied in the normal operation part of the output characteristic from no load up to maximum output current during normal operation. In this case the period time must be choosen so that the on time is larger than Tonmin so that during loadsteps Ton can be lowered. Below a certain Vout value (Voutlim in fig 3) the operating frequency will be lowered according to equation (4), assuming a fixed Vin.

$$Fphase = \frac{Vout}{Vin \cdot Ton} \qquad (4)$$

Fphase is the switching frequency of each phase. This means that the switching frequency will then be proportional to Vout. The internal oscillator that drives the switches operates at an N times higher frequency. The conversion factor 'a' in Fig 3 can be defined externally or kept fixed. In this case the current mode control loop operates as usual and will keep Ton almost constant. The blockdiagram and output characteristic using this function is given in fig 3: The current limit is realized by allowing a maximum peak current.

Also here at very low Vout the switching frequency is limited to a minimum value, to guarantee well defined switching behaviour.

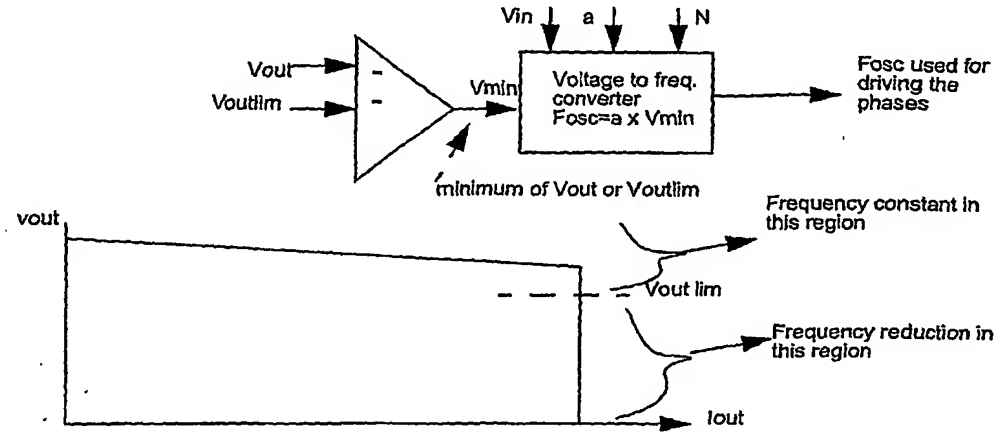

Fig 3. Frequency reduction at low Vout

Implementation 2 : make the frequency proportional to Vout over whole Vout region.

It is also possible to adapt the frequency over the whole Vout range. This is even simpeler because the Voutlim signal is not used. Adaption of the operating frequency over the loadline is probably not a disadvantage because only a slight frequency change occurs. This option is given in Fig 4

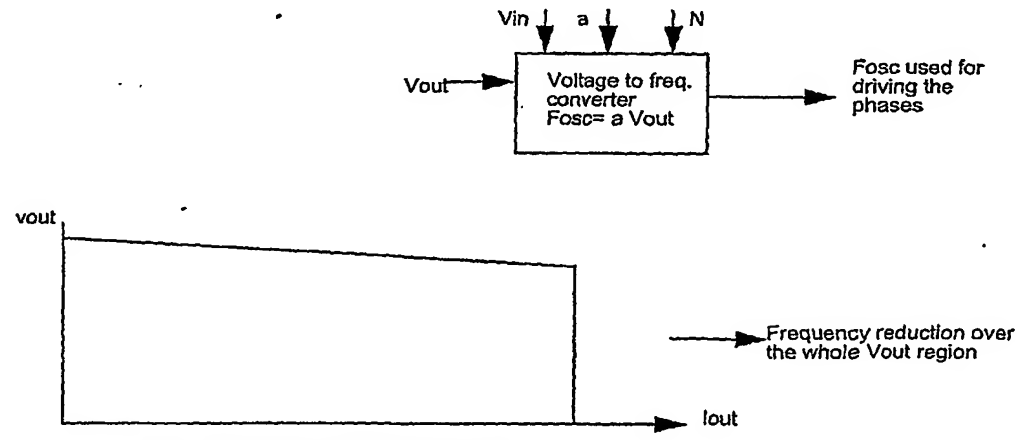

Fig 4. Frequency reduction at low Vout

Implementation 3 : Keep Ton constant over whole operation.

It is also possible to define the factor 'a' by a slow dynamic loop. This idea is given in Fig 5. The idea is that a desired on time is created that is a factor times the minimum on time. This factor can be fixed or externally tuned by a resistor. During operation the desired on time is compared with the actual on time and with a slow loop the factor 'a2' is adapated until

the desired on time occurs. As a result the operating frequency is automatically adapted to the maximum value possible at the given on time. The block N / Vin automatically compensates for variation of the switching frequency due to Vin variations and for the number of Phases. If Vin is fixed within certain limits or the number of phases is fixed this dependancy can be left out and then a2=a1.

Once a2 is determined it will not change because the switching frequency is determined according to equation (4).

The advantage of this solution is that always the operating frequency will be the maximum possible frequency under all circumstances and that it is not necessary to measure Vin accurately. If 5V or 12V operation is desired only 2 fixed values for Vin are sufficient because of the automatic adaption. Also the number of phases can be programmed internally in the VCO conversion factor.

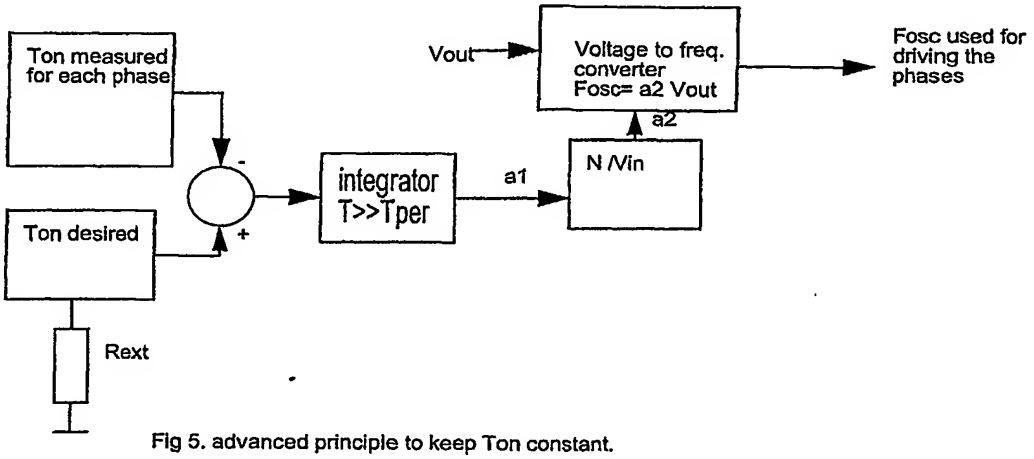

Fig 5. advanced principle to keep Ton constant.

ADVANTAGES OF THE INVENTION

-With the invention it is possible to minimize the ripple current in the main inductor. Therefore the output capacitors can be choosen as small as possible.

-The output voltage of the converter can be adapted over a very wide range without significant change in ripple current and with almost constant on time of the control fet. Constant on time of the control fet is an advantage because larger on-time variations caused by dynamic loadvariations are possible.

-No current sensing of the synfet current is necessary.

CLAIMS:

1. A power converter circuit of the buck converter type, wherein a period time depends on an output voltage of the power converter.

2. A power converter as claimed in claim 1, wherein the period time depends on a ratio between the output voltage and an input voltage of the power converter.

3. A power converter substantially as described herein with reference to the drawings.